

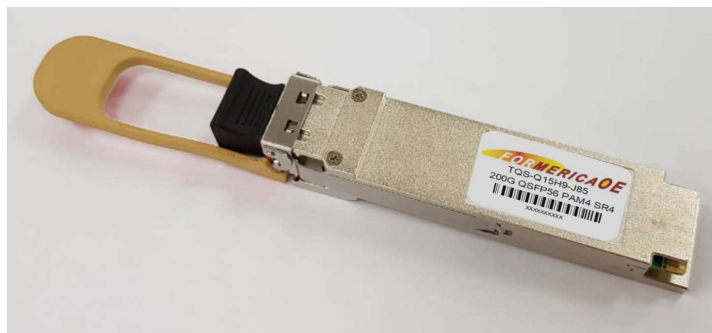
## Specification

**Quad Small Form-factor Pluggable  
(QSFP56)**

**Optical Transceiver Module**

**200G QSFP56 PAM4 SR4**

**(Preliminary)**



## Ordering Information

**T Q S – Q 1 5 H 9 – J 8 5**

Model Name	Voltage	Category	Device type	Interface	Temperature	Distance
TQS-Q15H9-J85	3.3V	With DDMI	850 nm VCSEL	CML/CML	0°C~+70°C	70m (OM3) 100m (OM4)

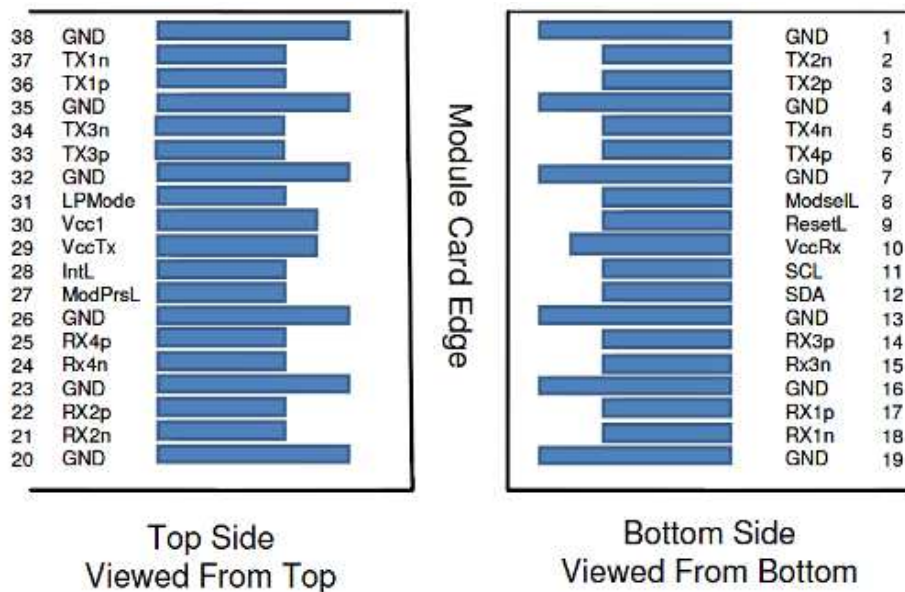
## Features

- Compliant with 100G Ethernet IEEE 802.3bm 100GBASE-SR4 standards
- Supports 200 Gbps data rate links of 70m/100m via OM3/OM4, respectively
- Hot pluggable electrical interface
- Using standard 12/8 lane optical fiber with MPO pluggable optical connector
- 0 to 70°C case temperature operating range
- RoHS Compliant (lead-free)

## Applications

- 200GBASE-SR4 Ethernet links.
- HPC Interconnects.
- Proprietary Interconnections.

Pin Descriptions



Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	
20		GND	Ground	1	
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	

24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	
30		Vcc1	+3.3V Power supply	2	
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	

### Absolute Maximum Rating

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Storage Temperature	Ts	-40		85	°C	
3.3V Power Supply Voltage	Vcc	-0.5		3.6	V	
Data Input Voltage-Single Ended		-0.5		V <sub>cc</sub> +0.5	V	1
Control Input Voltage		-0.5		3.6	V	
Relative Humidity	RH	5		85	%	
Rx Optical Damage Threshold / Lane		3.4			dBm	

#### Notes:

1. Non-condensing.

### Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0	55	70	°C	
Power Supply Voltage	3.135	3.3	3.465	V	
Data Rate per Channel		25.78125		Gb/s	
Bit Error Ratio		10 <sup>-12</sup>			
Control Input Voltage High	2		V <sub>cc</sub> +0.3	V	
Control Input Voltage Low	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate		100	400	kHz	
Differential Data Input / Output Load		100		Ohms	
Fiber Length: 2000 MHz.km 50/125um MMF (OM3)			70	m	
Fiber Length: 4700 MHz.km 50/125um MMF (OM4)			100	m	

**Electrical Characteristics**

Parameter	Min	Typical	Max	Unit	Note
<b>Transceiver Electrical Characteristics</b>					
TRx Power Consumption		TBD		W	
TRx Power-on Initialization Time			2000	ms	
<b>CAUI-4 Module Electrical Input Characteristics (TP1)</b>					
Signaling Rate per Lane	50			Gb/s	
Differential pk-pk input voltage tolerance			900	mV	
Differential termination mismatch			10	%	
Module stressed input test	Per Section 83E.3.4.1, IEEE 802.3bm				1
Single Ended Input Voltage Tolerance	-0.4		3.3	V	
DC common mode voltage	-350		2850	mV	
<b>CAUI-4 Module Electrical Output Characteristics (TP4)</b>					
Signaling Rate per Lane	50			Gb/s	
AC Common-Mode Output Voltage (RMS)			17.5	mV	
Differential Data Output Swing	400	600	800	mVpp	
Eye Width	0.57			UI	
Eye Height, Differential	228			mV	
Vertical Eye Closure			5.5	dB	
Differential termination mismatch			10	%	
Transition Time (20% to 80%)	12			ps	
DC Common Voltage	-350		2850	mV	

**Notes:**

1. The module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1, IEEE802.3bm. Module stressed input parameters include.
  - a. Eye width of 0.46 UI.
  - b. Applied pk-pk sinusoidal jitter is per Table 88-13 per IEEE802.3bm
  - c. Eye height of 95mV

**Optical Characteristics**

Parameter	Symbol	Min	Typical	Max	Unit	Note
<b>Transmitter Optical Characteristics</b>						
Signaling Rate per Lane		50			Gb/s	
Center Wavelength	$\lambda$	840	850	860	nm	
Spectral Width – RMS	$\Delta\lambda$		0.55		nm	
Average Launch Optical Power, each lane	LOP	-8.4		2.4	dBm	
Optical Modulation Amplitude, each lane	OMA	-6.4		3	dBm	
Launch power in OMA minus TDEC		-7.3			dBm	1
Transmitter and dispersion eye closure (TDEC), each lane	TDEC			4.3	dB	1
Average launch power of OFF transmitter, each lane				-30	dBm	
Extinction Ratio	ER	2			dB	
Optical return loss tolerance				12	dB	
Encircled Flux		$\geq 86\% @ 19\mu\text{m},$ $\leq 30\% \text{ at } 4.5\mu\text{m}$				1
Transmitter eye mask definition		$(X1, X2, X3, Y1, Y2, Y3) =$ $(0.3, 0.38, 0.45, 0.35, 0.41, 0.5)$				2

**Notes:**

1. Designed target and belonging to TDP for further confirmation.
2. Hit ratio  $1.5 \times 10^{-3}$  hits per sample

Parameter	Symbol	Min	Typical	Max	Unit	Note
<b>Receiver Optical Characteristics</b>						
Signaling Rate per Lane		50			Gb/s	
Center wavelength, each lane	$\lambda$	840	850	860	nm	
Damage Threshold		3.4			dBm	
Average power at receiver input, each lane		-10.3		2.4	dBm	1
Receiver Power, each lane (OMA)				3	dBm	
Receiver Reflectance				-12	dB	
Stressed receiver sensitivity in OMA				-5.2	dBm	
<b>Conditions of stressed receiver sensitivity test</b>						
Stressed eye closure (SEC)	SEC		4.3		dB	2
Stressed eye J2 Jitter	J2		0.39		UI	2
Stressed eye J4 Jitter,	J4			0.53	UI	2
OMA of each aggressor lane				3	dBm	2
Stressed receiver eye mask definition		(X1, X2, X3, Y1, Y2, Y3)= (0.28, 0.5, 0.5, 0.33, 0.33, 0.4)				3

**Notes:**

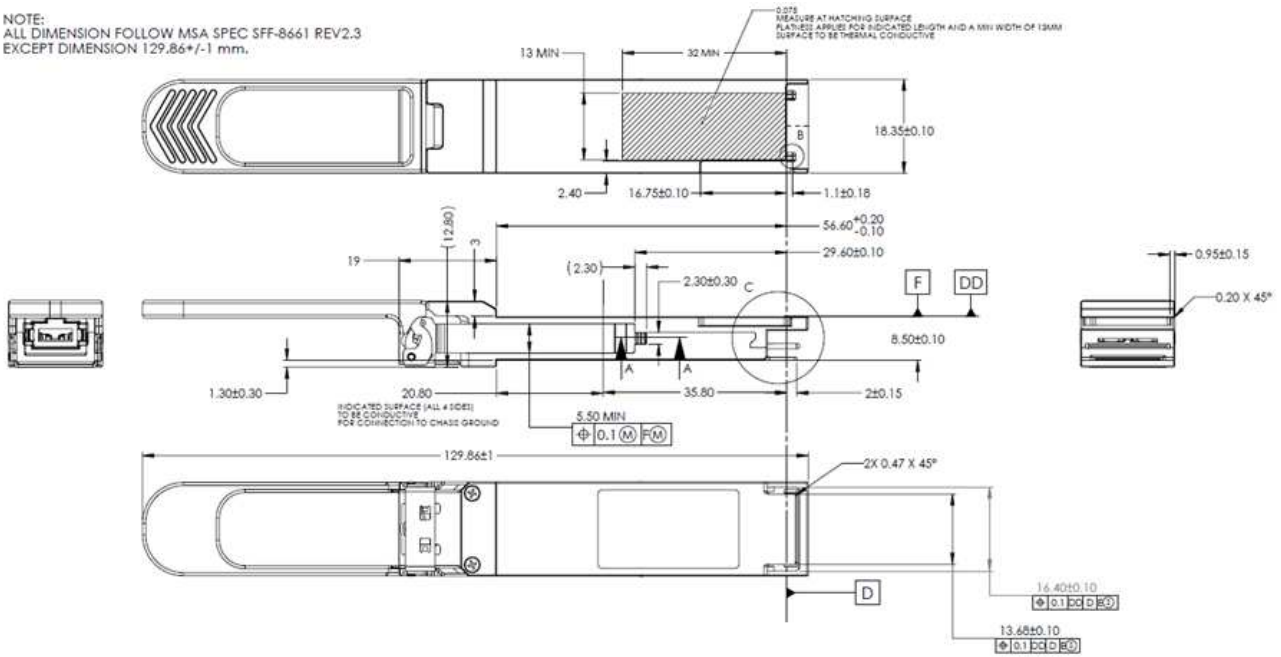
1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. TDP value and dependent parameters are subject to confirmation.
3. Hit ratio  $5 \times 10^{-5}$  hits per sample



Mechanical Design Diagram

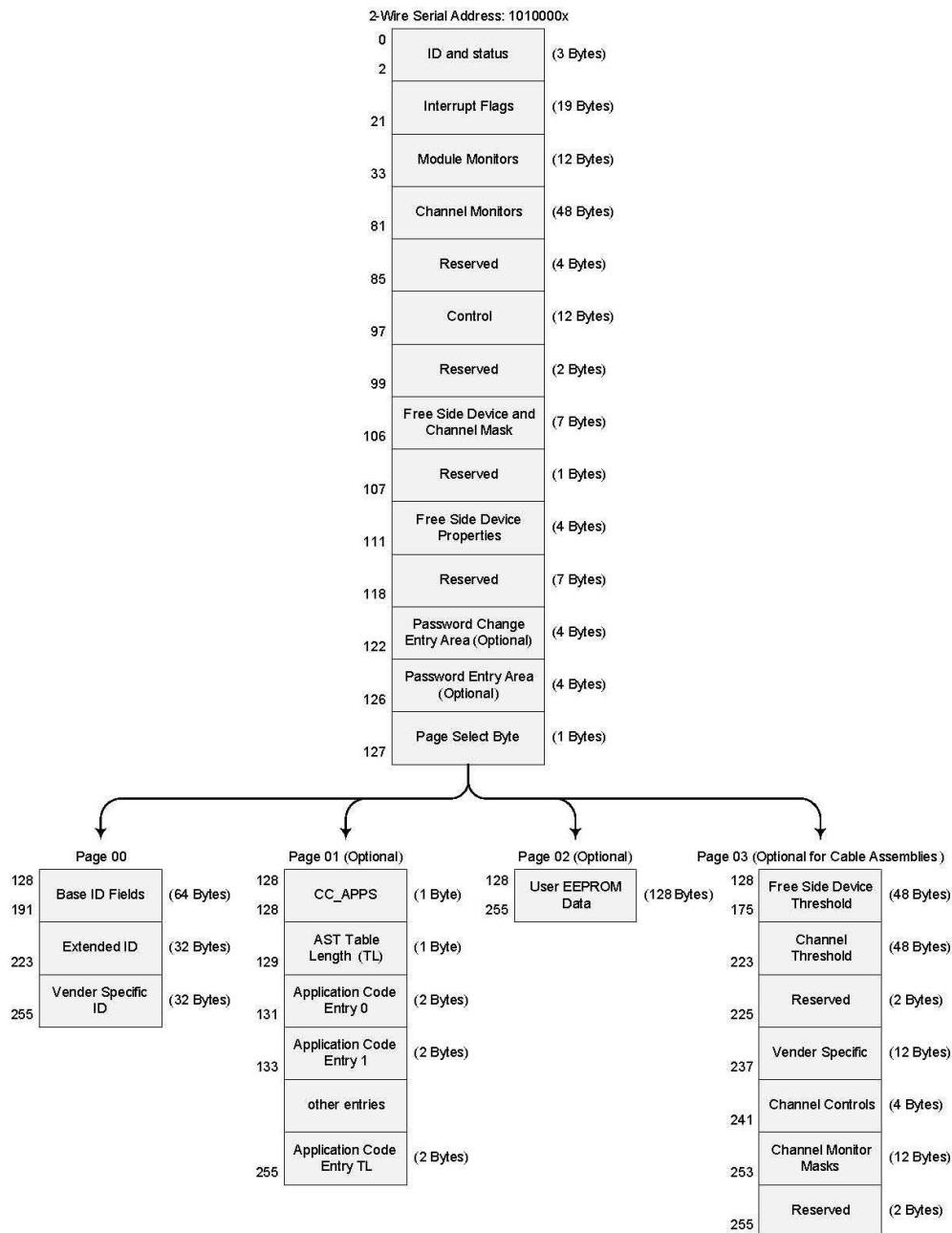
Unit: mm

NOTE:  
ALL DIMENSION FOLLOW MSA SPEC SFF-8661 REV.2.3  
EXCEPT DIMENSION 129.86+/-1 mm.



## Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP28 SFF-8636 MSA specification as shown in the below.



## ESD

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## User Manual

### **CAUTION**

Pull-Tab may shear off or snap if any one of the conditions are broken.

**1) Angular degree  $\leq 30^\circ$**

**2) Tensile strength  $\leq 60$  newton**

## Contact Information

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