Specification

Immersion Active Optical Cable

400G OSFP RHS Product

(Preliminary)

T E S – L 1 6 H 8 – P 8 M # #

Length (meter)

Ordering Information:

Model Name	TES-L16H8-P8M##	Note
Voltage	3.3V	
Device type	850nm VCSEL / GaAs PIN	
Interface	CML/CML	
Temperature	0°C ~ +70°C	
Latch Color	Beige	

Features

- Compliant with 400GAUI-4 specification
- Compliant CMIS 5.2
- Supports 425 Gbps aggregate bit rate
- Power consumption of max 9W per cable end
- Hot pluggable electrical interface
- RoHS Compliance
- IB and ETH support
- Compatible with immersion cooling liquid

Applications

- 400GBASE-SR4 400G Ethernet
- Data center

Absolute Maximum Rating

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Ts	-40	85	℃	
3.3V Power Supply Voltage	Vcc	-0.5	3.6	V	
Relative Humidity	RH	15	85	%	
Receiver Damage Threshold, per Lane	PRdmg	5		dBm	

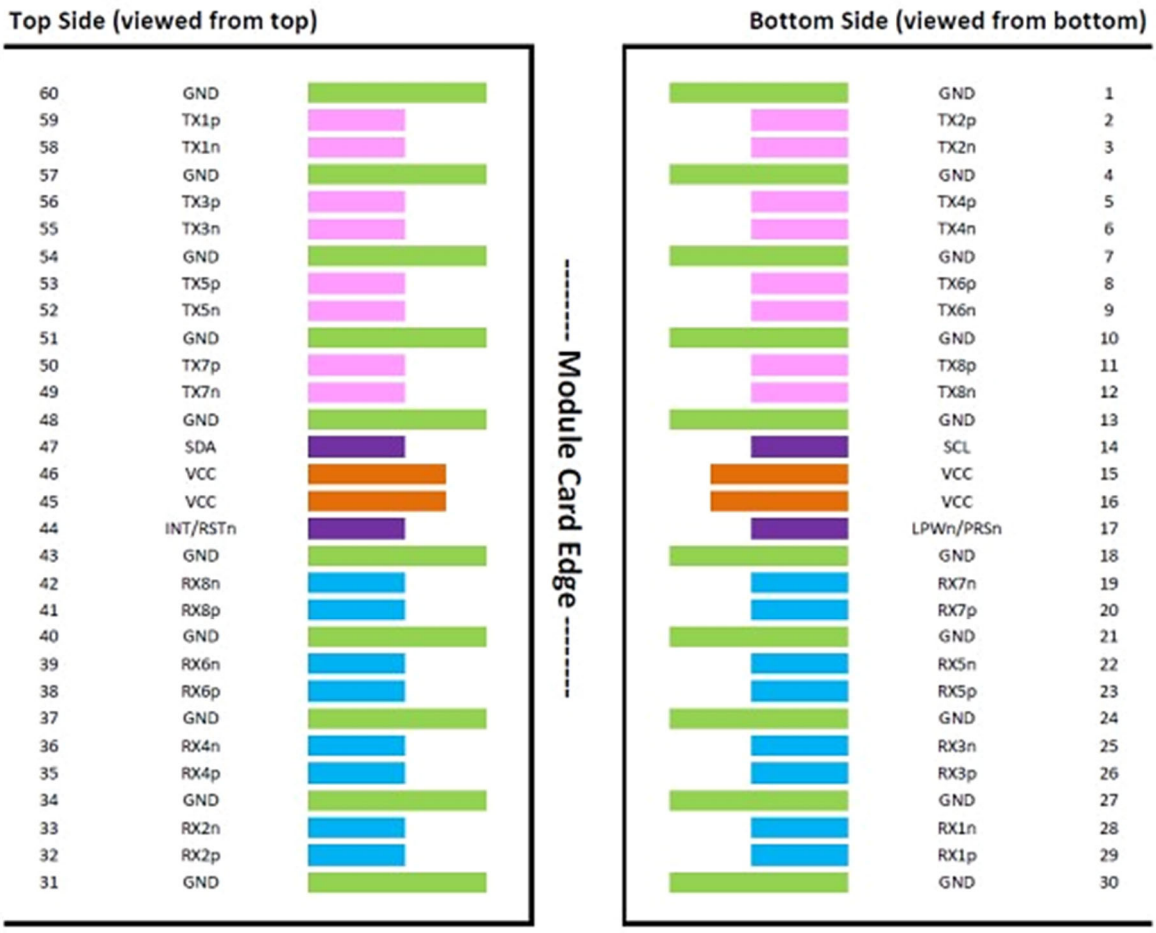
Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit	Note
Operating Case Temperature	0		70	℃	
Power Supply Voltage	3.135	3.3	3.465	V	
Total Power Consumption			9	W	
Supply Current per end			2.87	A	
Bit Rate			425	Gbps	
I2C Clock Frequency	0		1000	KHz	

Electrical Characteristics

Parameter	Min	Typ.	Max	Unit	Note
Pre FEC Bit Error Ratio			2.4E-4		
Post FEC Bit Error Ratio			1E-12		
Transmitter (each Lane)					
Differential pk-pk Input Voltage tolerance	750			mV	
Differential Termination Mismatch			10	%	
Eye height	10			mV	
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			dB	
Vertical eye closure			12	dB	
Effective return loss	7.3			dB	
Transition Time	10			ps	
Receiver (each Lane)					
Differential data output swing	300		900	mVpp	
Differential termination mismatch			10	%	
Eye height	15			mV	
Vertical eye closure			12	dB	
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G - 1)				
Effective return loss	8.5			dB	
Transition time	8.5			ps	

OSFP Module Pad Assignments and Descriptions

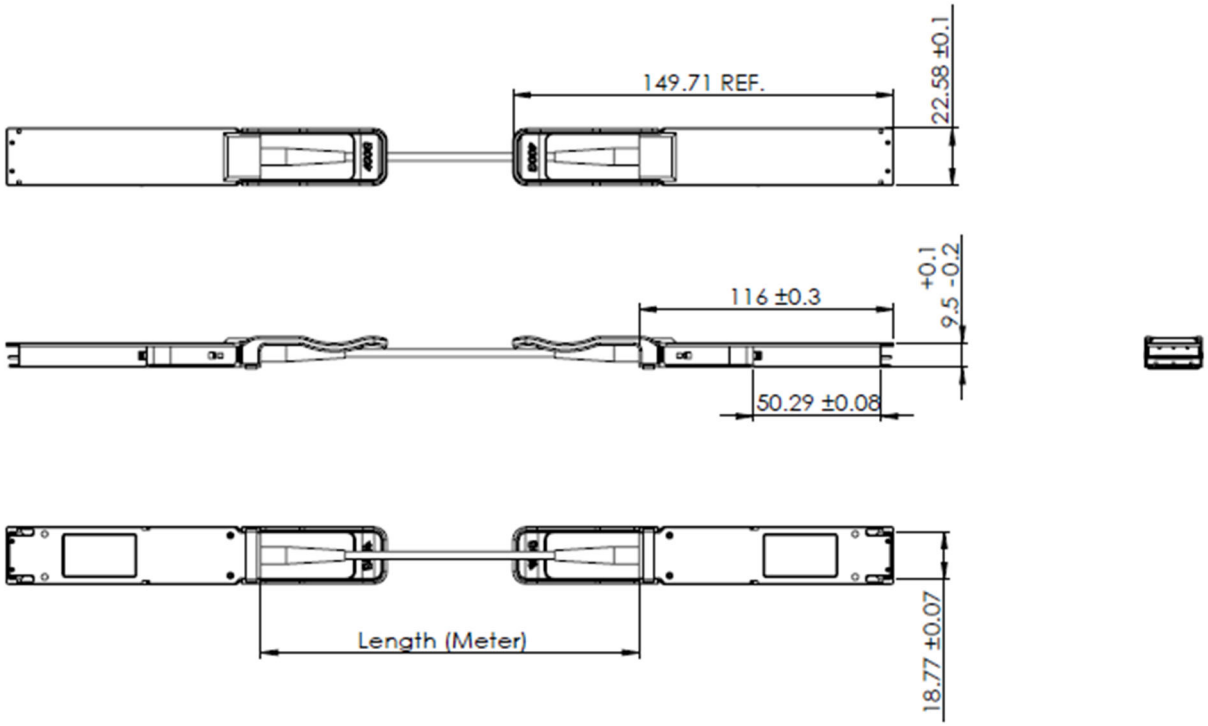


Pin	Logic	Symbol	Description	Plug Sequence	Notes
1	GND	*GND*	Ground	1	
2	CML-I	*Tx2p*	Transmitter Non-Inverted Data Input	3	
3	CML-I	*Tx2n*	Transmitter Inverted Data Input	3	
4	GND	*GND*	Ground	1	
5	CML-I	*Tx4p*	Transmitter Non-Inverted Data Input	3	
6	CML-I	*Tx4n*	Transmitter Inverted Data Input	3	
7	GND	*GND*	Ground	1	
8	CML-I	*Tx6p*	Transmitter Non-Inverted Data Input	3	
9	CML-I	*Tx6n*	Transmitter Inverted Data Input	3	
10	GND	*GND*	Ground	1	

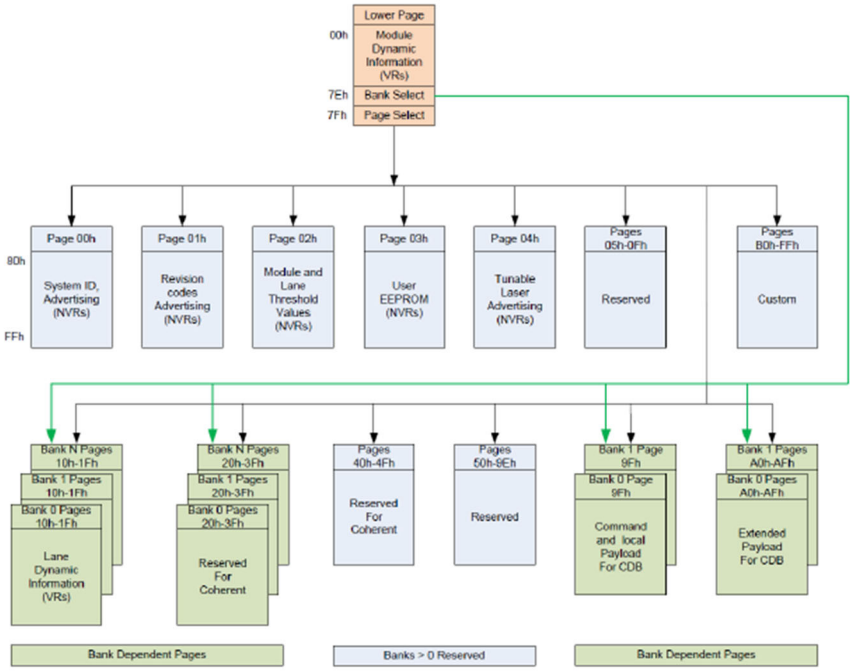
11	CML-I	*Tx8p*	Transmitter Non-Inverted Data Input	3	
12	CML-I	*Tx8n*	Transmitter Inverted Data Input	3	
13	GND	*GND*	Ground	1	
14	LVCOMS	*SCL*	2-wire Serial Interface Clock	3	Open-Drain with pull- up resistor on Host
15	VCC	*VCC1*	+3.3V Power Supply	2	
16	VCC	*VCC1*	+3.3V Power Supply	2	
17	Muti-Level	*LPWn/PRSn*	Low-Power Mode / Module Present	3	
18	GND	*GND*	Ground	1	
19	CML-O	*Rx7n*	Receiver Inverted Data Output	3	
20	CML-O	*Rx7p*	Receiver Non-Inverted Data Output	3	
21	GND	*GND*	Ground	1	
22	CML-O	*Rx5n*	Receiver Inverted Data Output	3	
23	CML-O	*Rx5p*	Receiver Non-Inverted Data Output	3	
24	GND	*GND*	Ground	1	
25	CML-O	*Rx3n*	Receiver Inverted Data Output	3	
26	CML-O	*Rx3p*	Receiver Non-Inverted Data Output	3	
27	GND	*GND*	Ground	1	
28	CML-O	*Rx1n*	Receiver Inverted Data Output	3	
29	CML-O	*Rx1p*	Receiver Non-Inverted Data Output	3	
30	GND	*GND*	Ground	1	
31	GND	*GND*	Ground	1	
32	CML-O	*Rx2p*	Receiver Non-Inverted Data Output	3	
33	CML-O	*Rx2n*	Receiver Inverted Data Output	3	
34	GND	GND	Ground	1	
35	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
36	CML-O	Rx4n	Receiver Inverted Data Output	3	
37	GND	GND	Ground	1	
38	CML-O	Rx6p	Receiver Non-Inverted Data Output	3	
39	CML-O	Rx6n	Receiver Inverted Data Output	3	
40	GND	GND	Ground	1	
41	CML-O	Rx8p	Receiver Non-Inverted Data Output	3	
42	CML-O	Rx8n	Receiver Inverted Data Output	3	
43	GND	GND	Ground	1	
44	Muti-Level	INT/RSTn	Module Interrupt / Module Reset	3	

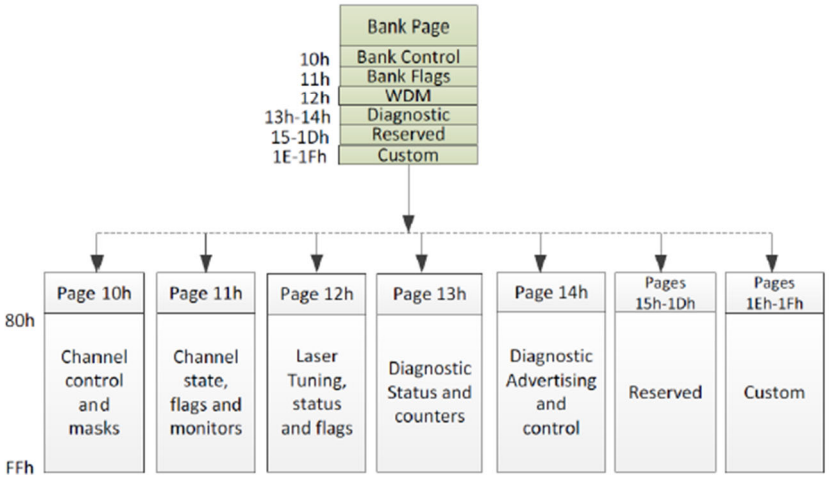
45	VCC	VCC1	+3.3V Power Supply	2	
46	VCC	VCC1	+3.3V Power Supply	2	
47	LVCMOS	SDA	2-wire Serial Interface Data	3	Open-Drain with pull-up resistor on Host
48	GND	GND	Ground	1	
49	CML-I	Tx7n	Transmitter Inverted Data Input	3	
50	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3	
51	GND	GND	Ground	1	
52	CML-I	Tx5n	Transmitter Inverted Data Input	3	
53	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3	
54	GND	GND	Ground	1	
55	CML-I	Tx3n	Transmitter Inverted Data Input	3	
56	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
57	GND	GND	Ground	1	
58	CML-I	Tx1n	Transmitter Inverted Data Input	3	
59	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
60	GND	GND	Ground	1	

Module Outline (Unit: mm)



Memory Map


Lower Page
00h
Module Dynamic Information (VRs)
7Eh
Bank Select
7Fh
Page Select
80h
FFh
Page 00h
System ID, Advertising (NVRs)
Page 01h
Revision codes Advertising (NVRs)
Page 02h
Module and Lane Threshold Values (NVRs)
Page 03h
User EEPROM (NVRs)
Page 04h
Tunable Laser Advertising (NVRs)
Pages 05h-0Fh
Reserved
Pages B0h-FFh
Custom
Bank N Pages 10h-1Fh
Bank 1 Pages 10h-1Fh
Bank 0 Pages 10h-1Fh
Lane Dynamic Information (VRs)
Bank N Pages 20h-3Fh
Bank 1 Pages 20h-3Fh
Bank 0 Pages 20h-3Fh
Reserved For Coherent
Pages 40h-4Fh
Reserved For Coherent
Pages 50h-9Eh
Reserved
Bank 1 Page 9Fh
Bank 0 Page 9Fh
Command and local Payload For CDB
Bank 1 Pages A0h-AFh
Bank 0 Pages A0h-AFh
Extended Payload For CDB
Bank Dependent Pages
Banks > 0 Reserved
Bank Dependent Pages


Bank Page
10h
Bank Control
11h
Bank Flags
12h
WDM
13h-14h
Diagnostic
15-1Dh
Reserved
1E-1Fh
Custom
80h
FFh
Page 10h
Channel control and masks
Page 11h
Channel state, flags and monitors
Page 12h
Laser Tuning, status and flags
Page 13h
Diagnostic Status and counters
Page 14h
Diagnostic Advertising and control
Pages 15h-1Dh
Reserved
Pages 1Eh-1Fh
Custom

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Revision History

Date	Version	Description
04/09/2024	0.1	Preliminary release
04/25/2024	0.2	Revised part number on the top of page