Specification

Quad Small Form Factor Pluggable Module 112

Optical Transceiver Pigtail

(Preliminary)

Ordering Information

T Q S – P 1 6 B B – P 8 M x x

Length

Ordering information:

Model Name	TQS-P16BB-X8Mxx	Note
Voltage	3.3V	
Device type	1310nm DFB	
Interface	CML/CML	
Temperature	0°C ~ +70°C	

Features

- Supports 425Gb/s aggregate bit rate
- Commercial case temperature range of 0°C to 70°C
- Single 3.3V power supply
- Maximum link length of 500m on single-mode Fiber (SMF)
- 4x100G PAM4 DFB-based 1310nm transmitter
- MPO-12 receptacles
- Hot-pluggable QSFP112 form factor
- Compliant with QSFP112 MSA.
- Compliant with IEEE 802.3bs 400GBASE-DR4
- Compliant with CMIS Rev. 5.0
- RoHS compliant
- Immersion Cooling Fluids Compatible

Application

- 400G Ethernet
- Other Optical Links
- Data Center and Enterprise Networking
- Immersion Liquid Cooling

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage temperature	Ts	-40	85	℃	
3.3V Power Supply voltage	Vcc	0	3.6	V	
Relative humidity (no-condensation)	Rh	0	85	%	
Damage Threshold	THd	5.5		dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Case Operating Temperature	Top	0		70	℃	
Power Supply voltage	Vcc	3.135	3.3	3.465	V	
Power Dissipation	Pd		10		W	
Link Distance		2		500	m	

Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
AC Common-mode output Voltage (RMS)				25	mV	
Differential output voltage long mode	-		-	845	mV	
Eye Height	EH	15			mV	
Vertical Eye Closure	VEC			12	dB	
Effective Return Loss	ERL	8.5			dB	
DC Common-mode Voltage Tolerance	-	-0.35		2.85	V	
Differential Termination Mismatch	-	-	-	10	%	
Receiver						
Differential Input Voltage Tolerance (TP1a)	-	750	-		mV	
AC Common-mode RMS Voltage Tolerance	-	25			mV	
Effective Return Loss	ERL	8.5			dB	
Single-ended Voltage	-	-0.4		3.3	V	

Tolerance Range						
DC Common-mode Voltage Tolerance	-	-0.35		2.85	V	
Differential Termination Mismatch	-	-	-	10	%	

Optical Characteristics

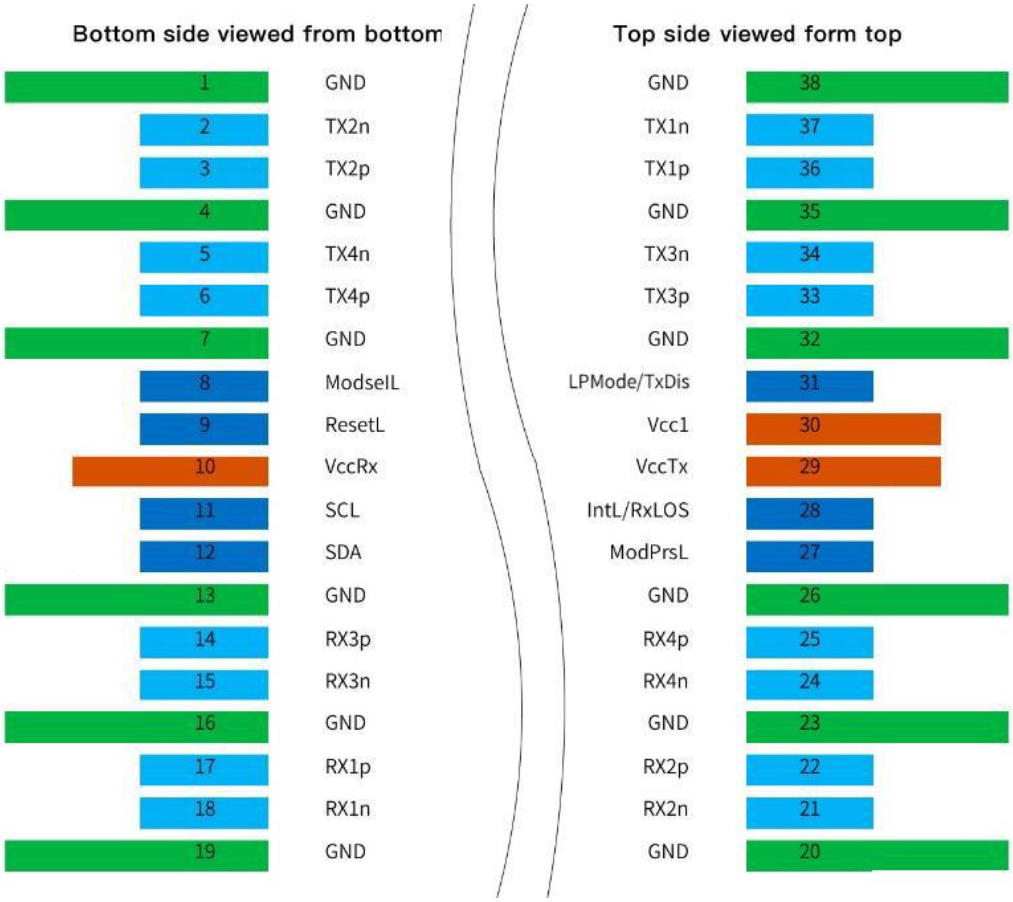
Parameter	Symbol	Min	Typ	Max	Unit	Note
Data Rate (each lane)		53.125 ± 100 ppm			GBd	
Center wavelength		1304.5	1310	1317.5	nm	
Transmitter						
Side-mode suppressizon ratio	SMSR	30			dB	
Average launch power, each lane	P_{AVG}	-2.9		4	dBm	1
Outer optical modulation amplitude (OMA_{outer}) each lane	P_{OMA}	-0.8		4.2	dBm	
ER < 4.5dB ER ≥ 4.5dB		TEDCQ 2.2				
Transmitter and Dispersion penalty, each lane	TDECQ			3.4	dB	
Extinction ratio, each lane		3.5			dB	
Average launch power of OFF transmitter				-15	dB	
Optical Return Loss Tolerance				21.4	dB	
Transmitter Reflectance[2]	RL			-26	dB	
Average Launch Power OFF Transmitter, each lance	P_{off}			-15	dBm	
$RIN_{21.4}$ OMA	RIN			-136	dB/Hz	
Receiver						
Center wavelength	λ	1304.5		1317.5	nm	
Damage threshold (min)		5			dBm	
Average receive power, each lane[2]		-5.9		4	dBm	1
Receive power (OMA_{outer}), each lane				4.2	dBm	
Receiver reflectance				-26	dB	

Receiver sensitivity (OMA_{outer}), each lane		Max(-3.9 SECQ-5.3)			dBm	
Stressed receiver sensitivity (OMA_{outer}), each lane (max) [3]	SRS			-1.9	dBm	
Transmitter Reflectance				-26	dB	
LOS Assert	LOSA	-30		-12.5	dBm	
LOS De-Assert	LOSD			-9.5	dBm	
LOS Hysteresis	LOSH	0.5			dBm	
Conditions of Stress Receiver Sensitivity Test						
Stressed eye closure for PAM4 (SECQ), lane under test			3.4		dB	
SECQ-10*$\log^{10}$(Ceq), Lane under test				3.4	dB	
OMAouter of each aggressor lane			4.2		dBm	

Note:

1. Average launch (receive) power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter Reflectance is defined looking into the transmitter.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lance.
4. Measure with conformance test signal at TP3 for the BER specified in IEEE Std 802.3cd.
5. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics s of power

QSFP112 Module Pad Assignments and Descriptions



Pin	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	3
9	LVTTL-I	ResetL	Module Reset	3
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3
12	LVCMOS-I/O	SDA	2-wire serial interface data	3
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3

16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3
18	CML-O	Rx1n	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	3
28	LVTTL-O	IntL/RxLOS	Interrupt	3
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode/TXDis	Low Power Mode , active high	3
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3
37	CML-I	Tx1n	Transmitter Inverted Data Input	3
38		GND	Ground	1

Function Description:

1. **Electrical interface:** All signal interfaces are compliant with the QSFP-112 MSA specifications. The high speed DATA interface is differential AC-coupled internally and can be directly connected to a 3.3V SERDES IC. Hardware control and status reporting pins include a 2-wire serial interface (SCL and SDA) and five 3.3V LVTTL hardware signals (ModSelL, ResetL, LPMode, ModPrsL, and IntL). The 2-wire interface pins are 3.3V LVCOMS compatible. Hosts shall use pull-up resistor connected toVcc_host on each of the 2-wire interface SCL,SDA, and all low speed status outputs.

2. **ModSelL:** The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

3. **ResetL:** The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

4. **LPMode/TxDis:** LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the TWI except during the execution of a reset. When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits the host controls how much power a module can consume. When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters. Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state (Power Override control bits) with transmitters already enabled, the module shall disable all optical transmitters. Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low, simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits

5. **ModPrsL**: ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

6. **IntL/RxLOS**: IntL/RxLOS is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change. If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. “high” indicates that there is no loss of received optical power. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.

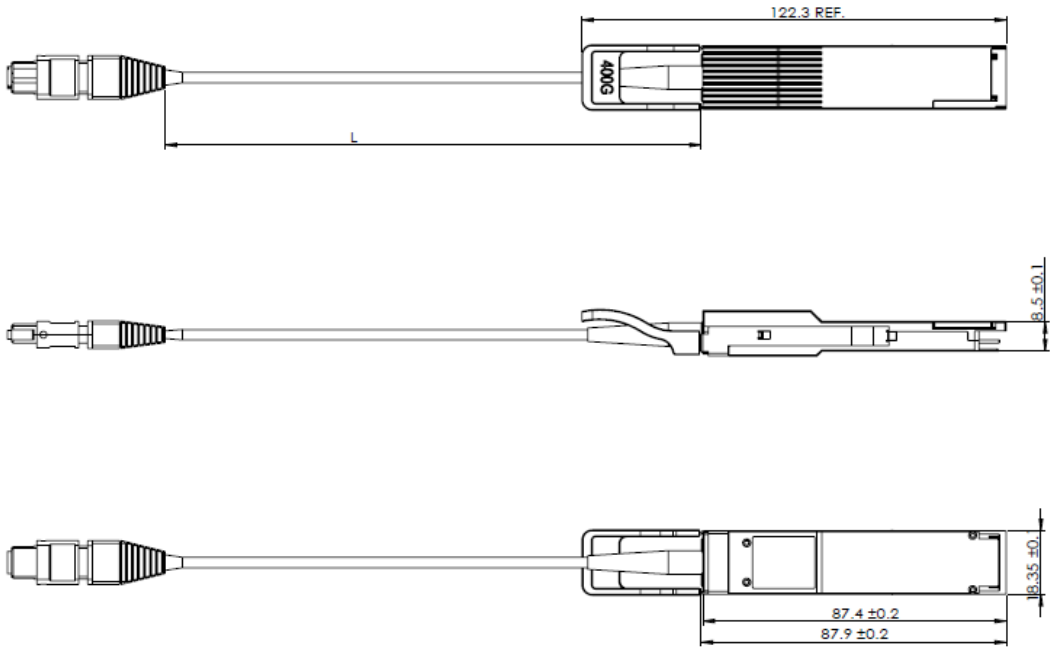
Digital Diagnostic Memory Map

Lower Memory Overview

Address	Size	Subject Area	Description
0-2	3	Management Characteristics	Basic Information about how this module is managed
3	1	Global Status Information	Current state of Module, Interrupt signal status
4-7	4	Flags Summary	Summary of Flags set on specific Pages (and Banks)
8-13	6	Module-Level Flags	Flags that are not lane or Data Path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or Data Path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering ModuleFault state
42-63	22	-	Reserved[22]
64-84	21	-	Custom[21]
85-117	33	Supported Applications Advertising	Applications supported by module Data Path(s)
118-125	8	Password Facilities	Password Entry and Change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable Upper Memory

Mechanical Dimension

(Unit: mm)



Digital Diagnostic

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	℃	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-3	3	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-3	3	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

ESD

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

LASER Safety

This is a Class 1 Laser Product according to IEC/EN60825-1:2014 (Third Edition). This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 56, MAY 8, 2019.
Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.
Attention: L'utilisation de commandes ou de réglages ou l'exécution de procédures autres que celles spécifiées dans le document peut entraîner une exposition à des radiations dangereuses.

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Revision History

Date	Version	Description
12/19/2023	0.1	Preliminary release
04/22/2024	0.2	Update format