

Specification

Quad Small Form-Factor Pluggable 56

Optical Transceiver AOC


200 Gigabit

Ethernet

TQS-Q15H8-XCZ##

Length
(meter)

Ordering Information:

Model Name	TQS-Q15H8-XCZ##	Note
Voltage	3.3V	
Device type	850 nm VCSEL	
Interface	CML/CML	
Temperature	0°C ~ + 70°C	
Latch Color	Beige 	

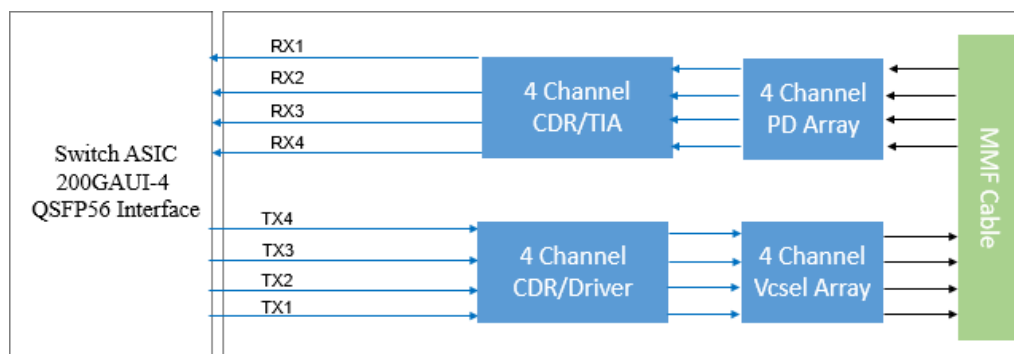
Features

- 4x50G PAM4 retimed 200GAUI-4 electrical interface
- 4 channel VCSEL arrays and 4 channels PIN photo detector arrays
- Maximum link length up to 100m
- Hot Pluggable QSFP56 to QSFP56 Form Factor AOC
- Complaint with SFF-8636 or Complaint with CMIS 5.2
- Compliant with IEEE 802.3cm
- Low power consumption < 4 W per cable end
- Single 3.3V power supply.
- I2C management interface
- Operating case temperature 0~70°C
- RoHS compliant 2.0

Applications

- Applicable to 200G Ethernet.
- Data center and in-rack connection.
- Enterprise networking
- InfiniBand HDR

Functional Block Diagram (Each end)



Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Relative Humidity (Non - condensing)	RH	15	85	%
Power Supply Voltage	Vcc	-0.5	3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Case Temperature	Top	0		70	°C
Power Supply Voltage	Vcc	3.135	3.300	3.465	V
Power Consumption per end ¹	P_dis	-	-	4	W
Supply Current per end				1.276	A
Bit Rate	BR			212.5	Gb/s
I2C Clock Frequency		0		400	kHz

Notes:

1. Under condition of 3.465V operating supply voltage, and 70°C case temperature.

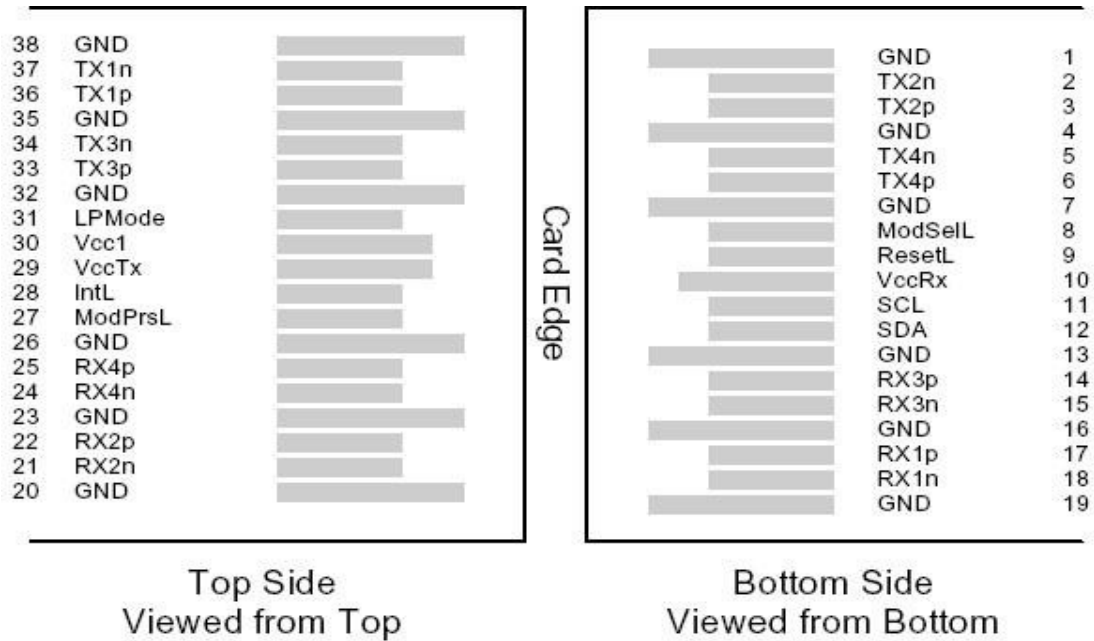
Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Data rate per lane		26.5625 ± 100ppm			Gbd	PAM4
Differential data input voltage per lane		900			mV	1
Differential input return loss		Pre equation (83E-5) IEEE802.3bm			dB	
Differential to common mode input return loss		Pre equation (83E-6) IEEE802.3bm			dB	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode voltage		-350		2850	mV	2
Receiver						
Data rate per lane		26.5625 ± 100ppm			Gbd	PAM4
AC common-mode output voltage (RMS)				17.5	mV	
Differential output voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)			0.265		UI	
Near-end Eye height, differential (min)		70			mV	
Far-end ESMW (Eye symmetry mask width)			0.2		UI	
Far-end Eye height, differential (min)		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss		Pre equation (83E-2) IEEE802.3bm			dB	
Common to differential mode conversion return loss		Pre equation (83E-3) IEEE802.3bm			dB	
Differential termination mismatch				10	%	
Transition time (min, 20% to 80%)		9.5			ps	
DC common mode voltage (min)		-350		2850	mV	2

Notes:

1. With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle
2. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage

Pin Description



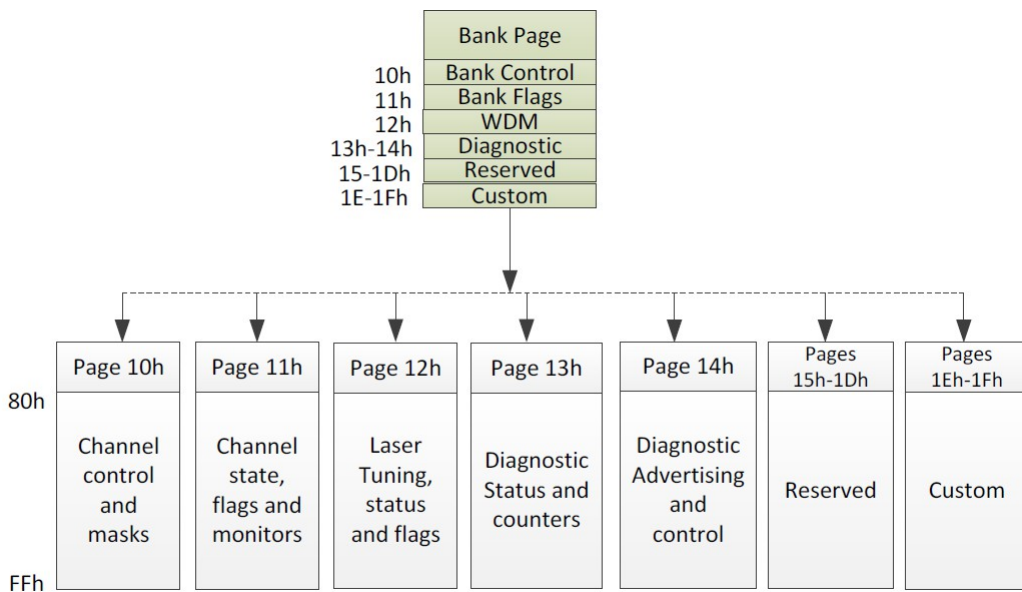
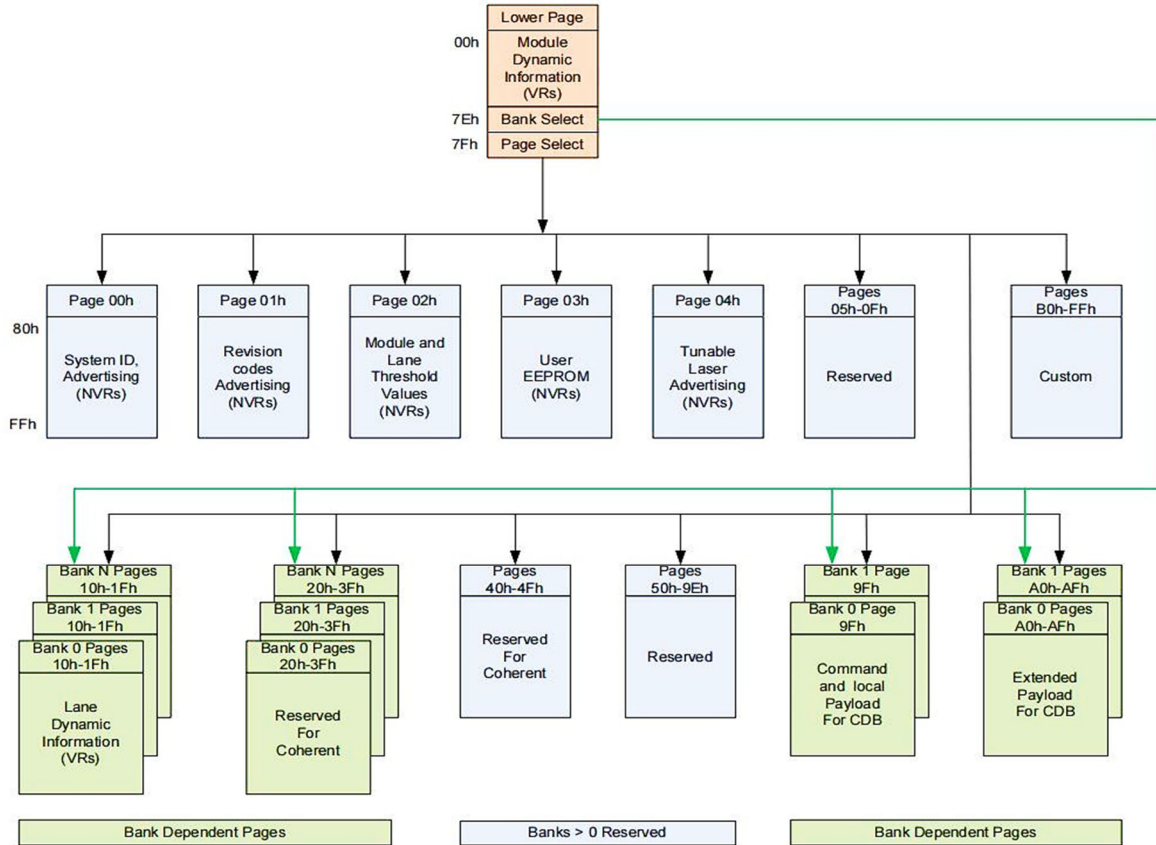
Pin	Name	Logic	Description	Power Seq.	Notes
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVC MOS-I/O	2-wire serial interface clock	3B	
12	SDA	LVC MOS-I/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	

16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3B	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsL	LVTTTL-O	Module Present	3B	
28	IntL	LVTTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMMode	LVTTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP56 modules. All are common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP56 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Memory Map



Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

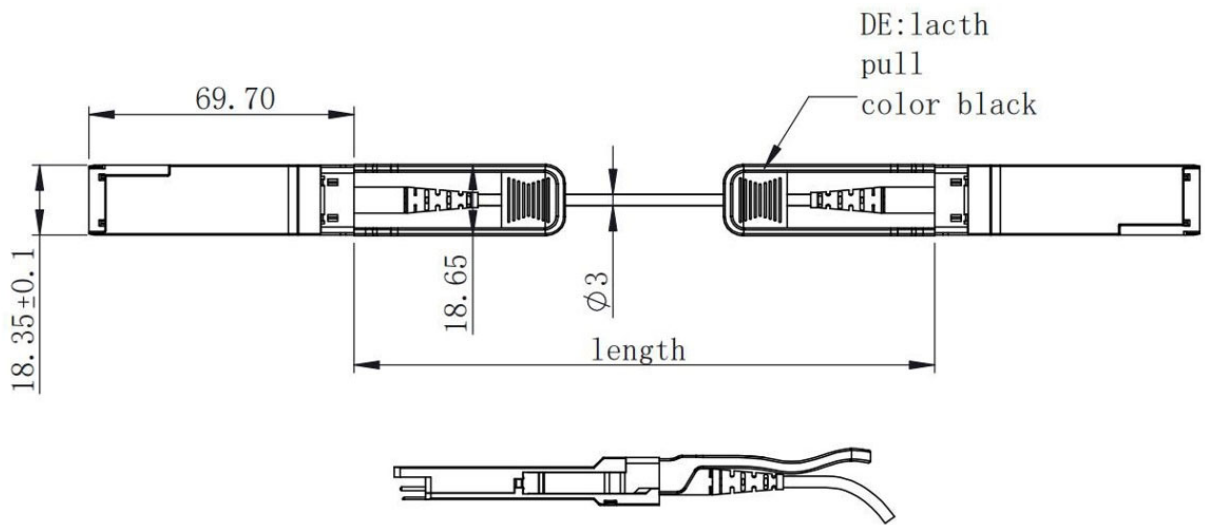
Parameter	Accuracy	Unit	Notes
Internally Measured AOC Temperature	±3	°C	1
Internally Measured AOC Supply Voltage	±3	%	
Measured Tx Bias Current	±10	%	
Measured Tx Output Power	±3	dB	2
Measured Rx Received Average Optical Power	±3	dB	

Notes:

1. Test point is the hotspot of the module.
2. DDM report stability shall be within 1 dB when temperature is stable. TX DDM must report -40 dBm when TX disable.

Module Outline

Unit: mm



Unremarked tolerances ± 0.2mm

■ Contact Information

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■ Revision History

Date	Version	Description
04/17/2024	0.1	Preliminary Release