Specification

Quad Small Form-factor Pluggable Double Density

Optical Transceiver Module

400G QSFP-DD PAM4 SR8

Ordering Information

TQS–R167A-883

Model Name	Voltage	Category	Device type	Interface	Temperature	Distance	Latch Color
TQS-R167A-883	3.3V	With DDMI	850 nm VCSEL	CML/CML	0°C~+70°C	70m (OM3) 100m (OM4)	Beige

Features

- Hot-pluggable QSFP-DD form factor
- Support 400G bps aggregate bit rates
- Up to 53.125G bps Data rate per channel
- Maximum link length of 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF
- MPO-16 APC connector receptacle
- Case temperature range(not environment): 0 ~ +70℃
- Power dissipation: <9W
- Single 3.3V power supply

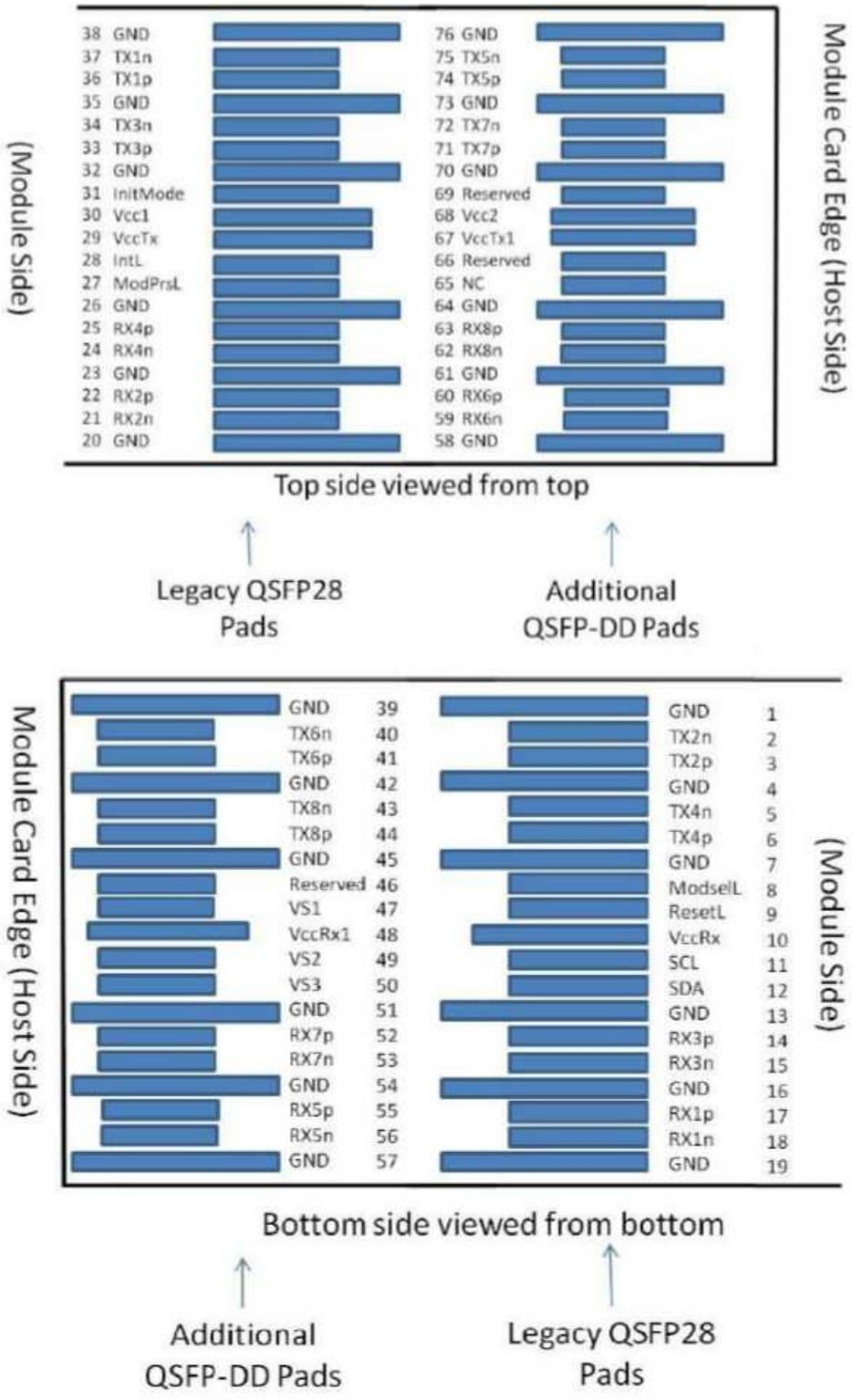
Applications

- 400G Ethernet
- Other Optical Links.

General Description

TQS-R167A-883 is a hot-pluggable QSFP-DD transceiver for 400G links over multimode fiber. It is high performance module for short-range data communication and interconnect application which operate at 400Gbps up to 70m using OM3 multimode fiber or 100m using OM4 multimode fiber. This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 76 pins connector. The optical interface uses MPO connector.

■ QSFP28 Module Pad Assignments and Descriptions



Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	

32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3

66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. **QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.**

2. **VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.**

3. **All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.**

4. **Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see above Figure for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.**

■ Absolute Maximum Rating

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Storage Temperature	Ts	-40		85	℃	
3.3V Power Supply Voltage	Vcc	-0.4		3.6	V	
Relative Humidity	RH	5		85	%	

■ Recommended Operating Conditions

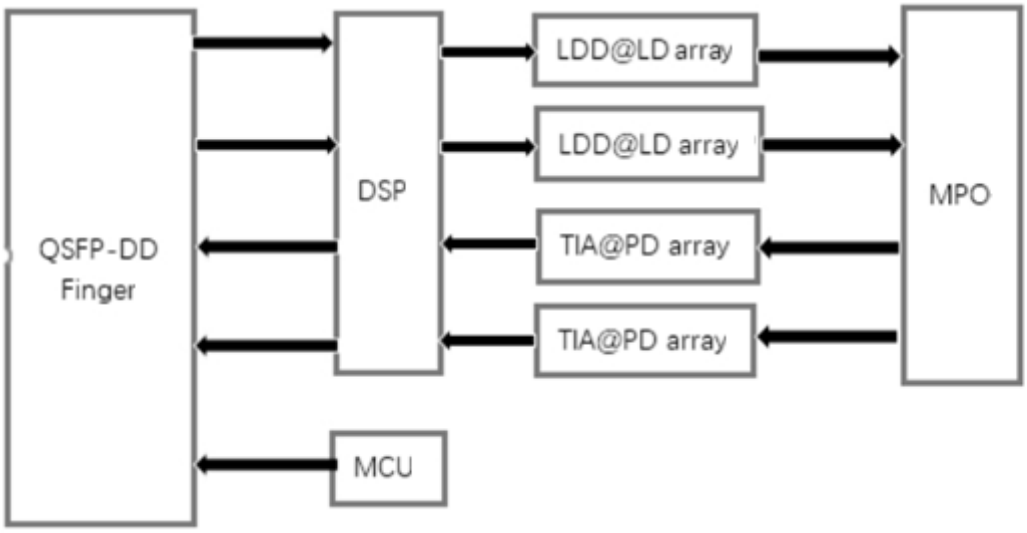
Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0		70	℃	
Power Supply Voltage	3.135	3.3	3.465	V	
Supply Current			2750	mA	
Bit Rate	424.96			Gbps	
Fiber Length onOM3 MMF			70	m	
Fiber Length on OM4 MMF			100	m	

■ Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			2750	mA	
Transmitter						
Input differential	Rin		100		Ω	1
Differential data input	Vin,pp	400		900	mV	
Receiver						
Differential data output	Vout,pp			900	mV	2

Optical Module Block Diagram



■ Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter Optical Characteristics						
Signaling Rate per Lane		26.5625±100ppm			GBd	
Modulation format		PAM4				
Center Wavelength	λ	840	850	860	nm	1
Spectral Width – RMS	Δλ			0.6	nm	
Average Launch Optical Power, each lane	LOP	-6.5		4	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	OMA	-4.5		3	dBm	
Launch power in OMAouter minus TDECQ (min)		-5.9			dBm	2
Transmitter and dispersion eye closure (TDECQ),each lane (max)	TDECQ			4.5	dB	
Average launch power of OFF transmitter, each lane				-30	dBm	
Extinction Ratio, each lane	ER	3			dB	
Optical return loss tolerance				12	dB	

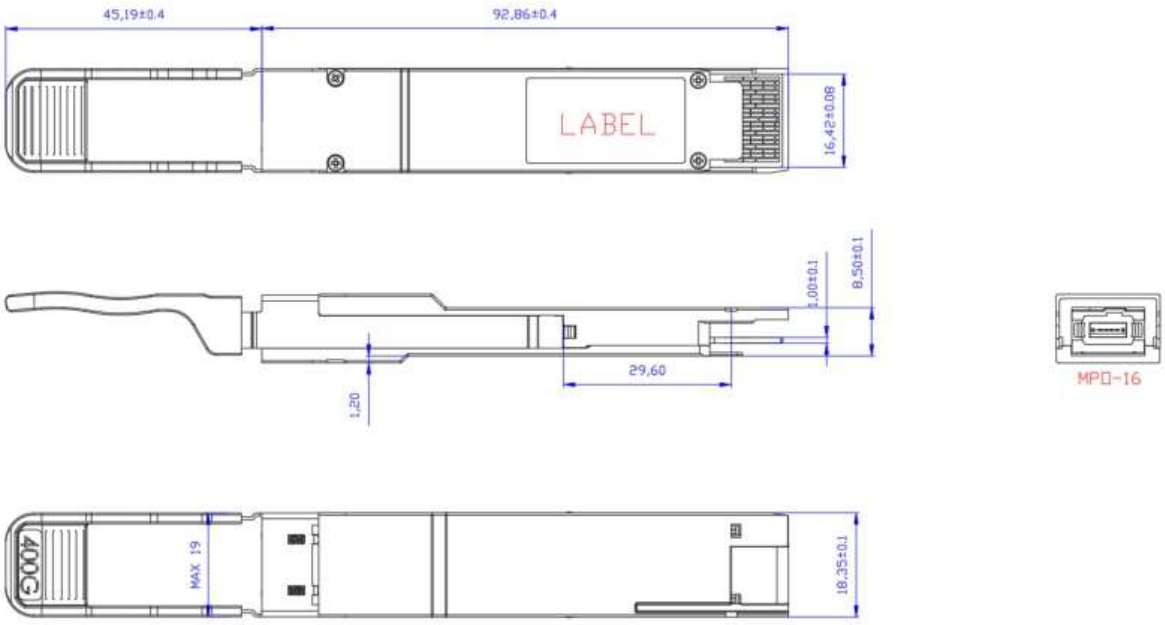
Parameter	Symbol	Min	Typical	Max	Unit	Note
Receiver Optical Characteristics						
Signaling Rate per Lane			26.5625± 100 ppm		GBd	
Modulation format			PAM4			
Center wavelength, each lane	λ	840	850	860	nm	
Damage Threshold		5			dBm	3
Average receiver power, each lane		-8.4		4	dBm	4
Receiver Power, each lane (OMAouter)				3	dBm	
Receiver Reflectance				-12	dB	
Stressed receiver sensitivity (OMAouter), each lane				-3.4	dBm	
Receiver sensitivity (OMA outer), each lane (max)		RS = max (-6.5 , SECQ – 7.9)			dB	5
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under			4.5		dB	6
OMA outer of each aggressor lane			3		dBm	6

Notes:

1. **RMS spectral width is the standard deviation of the spectrum.**
2. **Even if the TDECQ < 1.5 dB, the OMA (min) must exceed this value.**
3. **The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.**
4. **Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.**
5. **Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5 dB.**
6. **These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.**

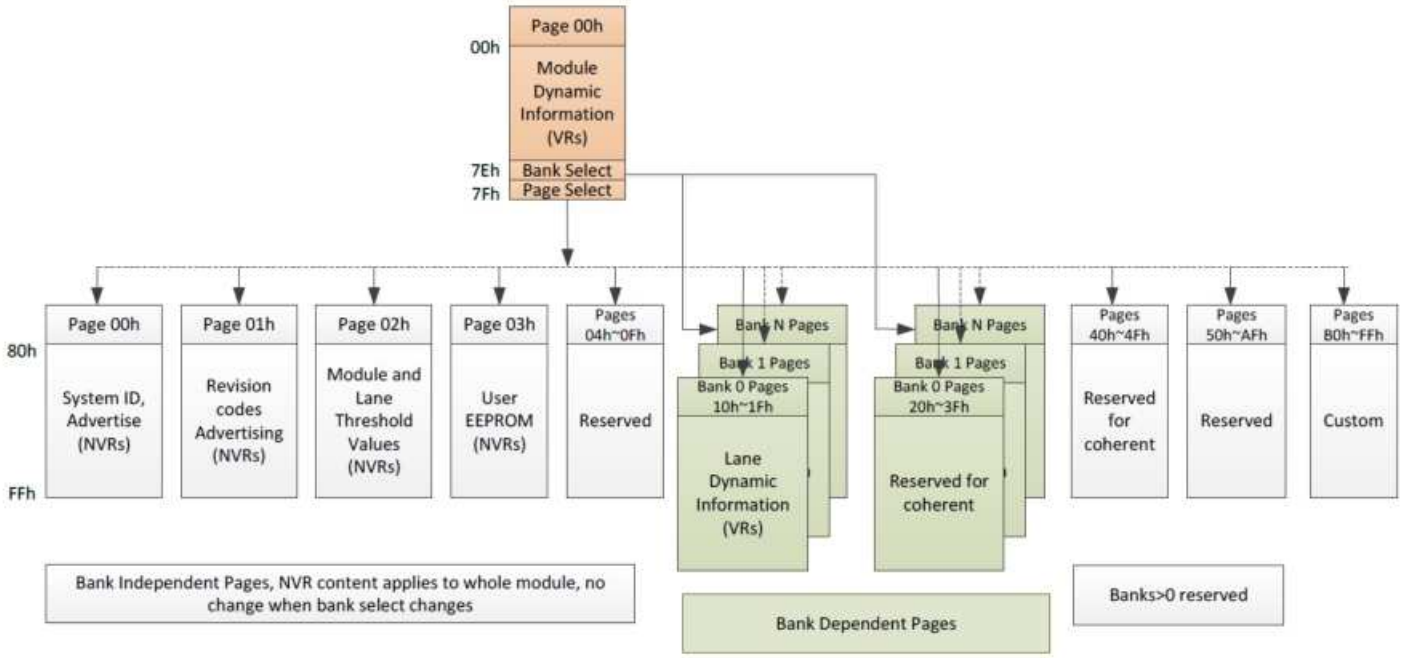
■ Mechanical Design Diagram

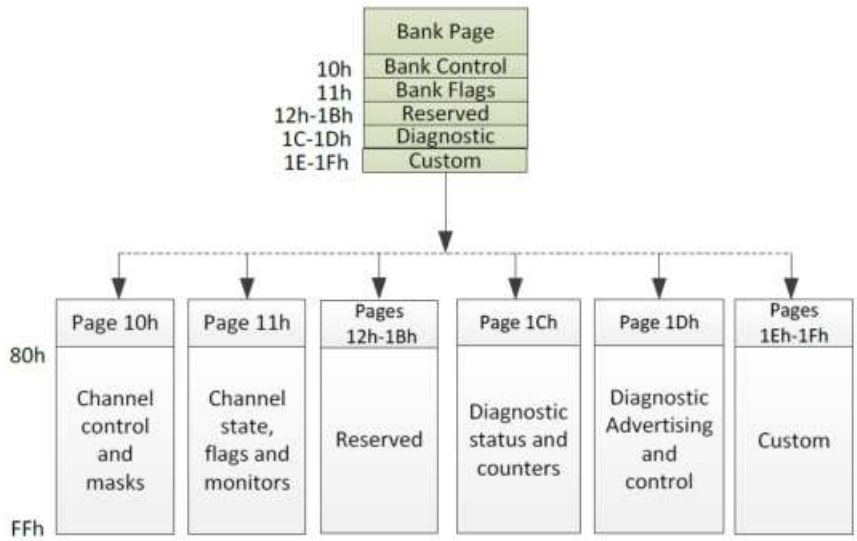
Unit: mm



■ Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP DD rev.3.0 specification as shown in the below (CMIS-4). For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.





■ Revision History

Date	Version	Description
05/18/2022	Preliminary	Preliminary version.